FULL PAPER

An Electrically Tuned Solid-State Thermal Memory Based on Metal–Insulator Transition of Single-Crystalline VO_2 Nanobeams

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A solid-state thermal memory that can store and retain thermal information with temperature states as input and output is demonstrated experimentally. A single-crystal VO_2 nanobeam is used, undergoing a metal–insulator transition at ~340 K, to obtain a nonlinear and hysteresis response in temperature. It is shown that the application of a voltage bias can substantially tune the characteristics of the thermal memory, to an extent that the heat conduction can be increased ~60%, and the output HIGH/LOW temperature difference can be amplified over two orders of magnitude compared to an unbiased device. The realization of a solid-state thermal memory combined with an effective electrical control thus allows the development of practical thermal devices for nano- to macroscale thermal management.

1. Introduction

Solid-state electronic devices such as diodes and transistors form the cornerstone of modern electronic systems. Active devices provide the ability to control electron flow required to realize basic functional building blocks such as amplifiers, logic gates, and memories. However, practical counterpart solid-state devices for active control of heat conduction and storage of thermal information are still not available, even though many theoretical proposals have been put forward.[1–3] For example, thermal rectification[1], thermal logic operations[2] and storage of thermal information[3] using heat have been put forward in theoretical models. Despite significant progress and refinement in such theoretical studies, the experimental demonstration of active and nonlinear thermal devices for control of heat remains a challenge. Unlike electrical conductance, which can be changed by more than a factor of 10^6 for a typical field-effect transistor, the thermal conductance shows only an 85% variation at best in a tunable thermal link.[4] The difficulty in modulating the heat conduction in real material system with external control is a major obstacle for the realization of practical functional solid-state thermal devices. Recently, nanoscale solid-state thermal rectifier and phonon waveguide have been demonstrated experimentally in carbon and boron nitride nanotubes,[5,6] which provided experimental validation that the phonons, like electrons and photons, can also be processed. Here, we demonstrate a practical solid-state thermal memory device that can store and retain thermal information with temperature states as input and output by exploiting the metal–insulator transition (MIT) of single-crystalline VO_2 nanobeams. We show that, under the control of a voltage bias across the VO_2 nanobeam, the thermal memory exhibits several large tunable features, including the enhancement of heat conduction, the amplification of the output temperature between the high and low states, and tuning of the operating temperature.

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2. Results and Discussion

Our thermal memory device consists of three basic segments: an input terminal (T_{in}), an output terminal (T_{out}), and a heat conduction channel bridging the two. The two terminals are suspended with suspension leads connected to the substrate (T_{base}) (**Figure 1**a). To explore the thermal memory effect, we used a single-crystalline suspended VO_2 nanobeam, which undergoes MIT from a low-temperature insulating (I) phase to a high-temperature metallic (M) phase around 340 K,[7] as a

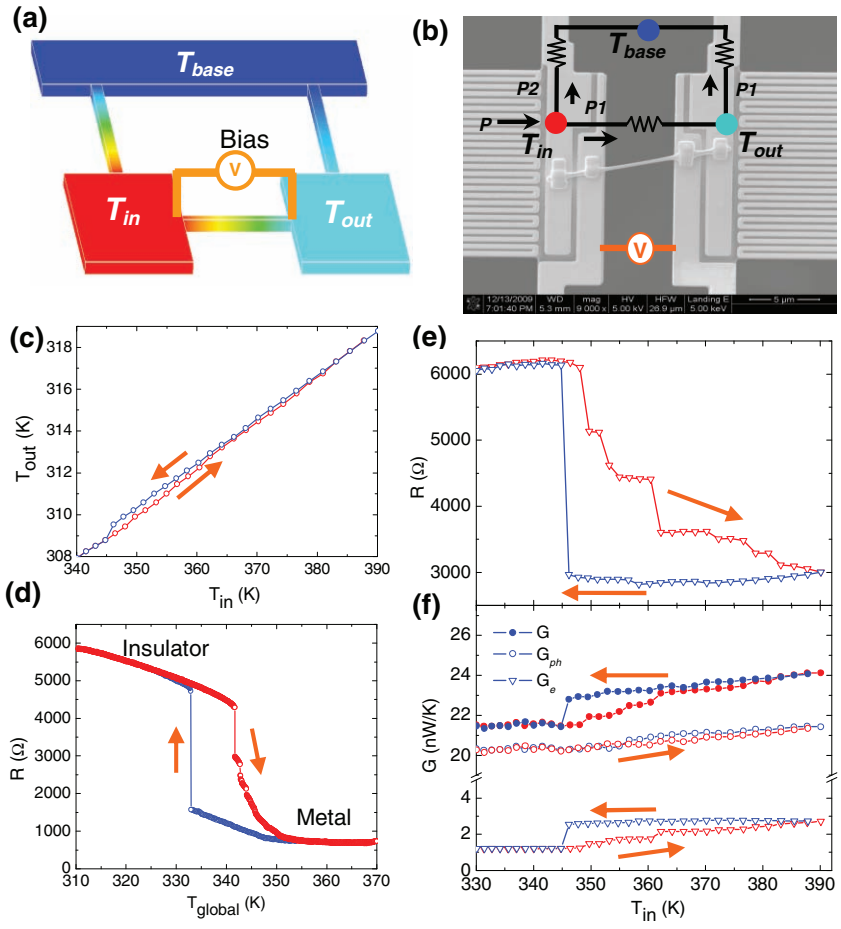

Figure 1. Solid-state thermal memory device with an individual VO_2 nanobeam as a thermal channel. (a) A schematic illustration of a thermal memory device. Contour colors indicate the temperature. (b) SEM image of a thermal memory device consisting of a VO_2 nanobeam connecting the input terminal (T_{in}, left side) and output terminal (T_{out}, right side). An equivalent thermal circuit is also depicted in the image. (c) T_{out} as a function of T_{in} of the thermal memory without the application of a voltage bias upon heating (red curve) and cooling (blue curve). For clarity, only data collected over a range with temperature hysteresis are shown. (d) Electrical resistance R of the nanobeam as a function of the global temperature with a uniform temperature distribution ($T_{global} = T_{in} = T_{out} = T_{base}$) upon heating (red curve) and cooling (blue curve). (e) Electrical resistance R of the nanobeam under a temperature gradient as a function of the input temperature T_{in} upon heating (red curve) and cooling (blue curve). (f) Total thermal conductance G, phonon contribution G_{ph} and electronic contribution G_e of the nanobeam as a function of T_{in} without the application of the voltage bias upon heating (red curve) and cooling (blue curve). Arrows on the curves denote the temperature sweep directions.

tunable thermal channel to obtain a nonlinear response between T_{in} and T_{out}. A voltage bias, applied across the VO_2 nanobeam, is used to tune the characteristics of the thermal memory.

Single-crystalline VO_2 nano- and micro-beams were synthesized using a catalyst-free chemical vapour deposition route. The details of the material characterization of the VO_2 nanobeams have been published elsewhere.[8] Individual VO_2 nanobeams were placed on a custom-designed suspended micro-electrothermal device using piezo-driven nanomanipulators operated inside a scanning electron microscope (SEM). Two ends of the nanobeam were bonded to four metal contacts by deposition of Pt-like film using a focused ion beam. Figure 1(b) shows an SEM image of a thermal memory device consisting of a single 150 nm wide and 5 μm long VO_2 nanobeam bridging two suspended SiN_x membranes, which are denoted as the input (T_{in}) and output (T_{out}) terminals, respectively. Each membrane, integrated with a Pt resistive loop that serves as both heater and temperature sensor, is suspended by six electrical leads on SiN_x beams tied to the substrate (Figure 1b and Supporting Information Figure S1). This construction allows us to simultaneously conduct thermal transport measurement based on a method described previously,[9] and four-probe electrical transport measurement of the nanobeam, thus directly correlating both thermal and electrical properties on the same sample. All the measurements were carried out in vacuum ($<10^{-5}$ mbar) at room temperature ($T_{base} = 300$ K).

We first examined the thermal memory effect of the VO_2 nanobeam without the application of a voltage bias. A heating power P was supplied to the input terminal T_{in} using the Pt resistive loop and was gradually changed to sweep T_{in} from 300 K to 390 K. As shown in the equivalent thermal circuit depicted in Figure 1b, part of heat, *P1,* is conducted through the nanobeam to the output terminal, raising the temperature of the latter T_{out} accordingly. *P1* is finally dissipated to the substrate T_{base} through the six beams supporting the output terminal. The balance, *P2,* of the heating power is conducted to the substrate T_{base} through the other six beams supporting the input terminal. By performing a forward and reverse sweep of T_{in} in the vicinity of MIT of VO_2, we observe that the ($T_{in} - T_{out}$) curve is non-linear and hysteretic (Figure 1c), i.e., the curve makes a loop rather than retrace its path for increasing and decreasing temperature, showing bi-stable (HIGH/LOW) temperature states at the same input temperature, which is an essential feature of the thermal memory.

To study the origin of this unique thermal memory effect arising from the MIT, we first measured the electrical resistance R of the VO_2 nanobeam with a uniform temperature distribution as a function of the global temperature ($T_{in} = T_{out} = T_{base}$) (Figure 1d). Upon heating, R shows an initial abrupt drop followed by several small steps that correspond to new M phases nucleating from the I phase.[10] When the temperature is increased to 354 K, the transition to the M phase is complete. During the cooling process, the entire nanobeam maintains a contiguous M phase above 333 K, and then transforms directly and in its entirety to the I phase at this temperature, exhibiting single-domain behaviour. It also shows that R is a highly hysteretic function of temperature upon the heating and cooling process in correspondence with the hysteretic MIT.

We then performed simultaneous thermal and electrical transport measurements of the nanobeam during repeated cycling of T_{in}. A small DC current of 200 nA was used in the measurement of the electrical resistance R. This magnitude of DC current did not introduce a detectable perturbation to the heat conduction characteristics, as repeated thermal measurements without the DC current produced essentially identical ($T_{in} - T_{out}$) curves as shown in Figure 1c. The electrical resistance R as a function of T_{in} is shown in Figure 1e. Similarly, upon sweeping T_{in}, the nanobeam exhibits stepwise transitions during heating and an abrupt transition upon cooling (Figure 1e). Unlike the uniform-temperature sweeps described above, here the transition to the M phase upon heating is not complete, with R (~3 kΩ) being 4 times larger than the value of the fully-metallic nanobeam, even when T_{in} is increased to 390 K. These observations can be understood by the incomplete phase transition of the VO_2 nanobeam caused by the non-uniform temperature distribution from the input terminal (390 K) to the output terminal (319 K). It has been observed that suspended VO_2 nanobeams show single-domain behavior during MIT, whereas substrate-supported VO_2 nanobeams contain periodic multiple M-I domains arising from the uniaxial strain imposed by elastic mismatch with the substrate.[10] In the thermal memory device, the VO_2 nanobeam is suspended between the input and output terminals, which is free from the substrate-induced strain. Under such circumstances, a single M domain preferentially nucleates from the I phase at the high temperature end when T_{in} reaches ~345 K, and then grows one dimensionally along the VO_2 nanobeam towards the low-temperature end with increasing temperature T_{in}. Large resistance steps indicate abrupt growth of the M domain during the forward heating sweep. Under repeated cycling in T_{in} from 300 K to 390 K, the abrupt transition from M phase to I phase upon cooling is reproducible over hundreds of cycles, suggesting strain-induced instability in domain formation is absent in our suspended devices.

Based on the temperature changes and the heating power P at the input terminal, the thermal conductance G of the nanobeam can be determined from the relation[9]

$$G = P\left(\frac{\Delta T_{out}}{\Delta T_{in}^2 - \Delta T_{out}^2}\right) \quad (1)$$

where ΔT_{in} and ΔT_{out} are the temperature changes relative to the base temperature (T_{base} = 300 K) at the input terminal and the output terminal, respectively. The measured thermal conductance G includes both phonon contribution, G_{ph}, and electronic contribution, G_e. The ability of quasiparticles to transport heat is given strictly by their ability to transport charge, as described by a universal relation known as the Wiedemann–Franz (WF) law.[11] The WF law is found to hold not only in simple metals like copper, but also in systems with strong electron correlations and in disordered inhomogeneous systems at the vicinity of MIT.[11c] To decouple phonon contribution and electric contribution of the VO_2 nanobeam during the MIT, the electronic contribution G_e is estimated from the WF law from the relation $G_e = LT/R$,[11a] where $L = 2.4 \times 10^{-8}$ WΩK^{-2} is the degenerate Lorentz number, T is the average temperature between T_{in} and T_{out}, and R is the electrical resistance of the beam obtained from four-point measurements. Consequently, the phonon contribution G_{ph} is derived from the total thermal conductance G by subtracting the electronic contribution G_e. As shown in Figure 1f, the phonon contribution dominates the heat conduction over the temperature range swept, with thermal conductance G_{ph} varying from 20.2 nW/K to 21.4 nW/K (middle curve), but its variation (<0.2 nW/K) at the same input temperature upon heating and cooling is small. In contrast to the large variation (~1.4 nW/K, 7% of the total thermal conductance) in the electronic contribution (G_e ~ 1.2 to 2.6 nW/K, bottom curve), the hysteresis arising from the phonon contribution is negligible. This observation is consistent with the thermal properties of VO_2 thin film on either side of the MIT as measured by time-domain thermoreflectance, in which the change in thermal conductivity is due to the electronic contribution.[12] Therefore, the mechanism underlying the bi-stable temperature states can be attributed mainly to the hysteresis in the electronic contribution to the heat conduction during the MIT of the VO_2 nanobeam.

Upon examining the thermal memory characteristics, we note that the temperature hysteresis loop is relatively small (output HIGH/LOW difference ~0.25 K at T_{in} = 360 K, Figure 1c). The application of an electrical bias across the suspended VO_2 nanobeam provides a powerful means to control the thermal profile of the nanobeam through Joule heating, thereby defining the characteristics of the thermal memory. We found that the application of a voltage bias leads to the single-domain behaviour, whereas the application of a current bias gives rise to the multi-domain behaviour, due to the different electrothermal feedback mechanism of the bias (Supporting Information Figure S2). To substantially enhance the output HIGH/LOW difference, a voltage bias is applied across the ends of the nanobeam to tune the characteristics of the thermal memory device.

Figure 2a shows the ($T_{in} - T_{out}$) curves upon sweeping of T_{in} under different voltage biases. Two important features of the thermal memory are remarkably altered with the voltage bias. First, the hysteresis loop is substantially enlarged and is shifted to lower temperatures with increasing voltage bias, lowering the operating temperature of the thermal memory (Supporting information Figure S3). Secondly, the difference in the output temperature T_{out} between the HIGH and LOW states (defined at T_{in} = 360 K) increases substantially with increasing voltage bias (blue curve, Figure 2b). In the heating sweep, an incremental increase in T_{in} can result in abrupt increases in both T_{in} and T_{out}, as M domains form which decreases the electric resistance of the beam, and which in turn increases the electrical current and Joule heating (V^2/R) in a positive electrothermal feedback cycle until a quasi-equilibrium M-I domain configuration and heating pattern is established in the nanobeam. Note that increased Joule heating of the nanobeam simultaneously affects both T_{in} and T_{out} as the heat is conducted to both terminals, and in this sense the input terminal T_{in} is not unaffected by the state of the memory. At 0.047 V (Figure 2a), at T_{in} = 368 K, the regenerative electrothermal feedback causes the VO_2 nanobeam to abruptly and fully transform into a metallic state, leading to abrupt increases in T_{in} and T_{out} to 400 K and 353 K, respectively. For lower biases, a fully metallic state is not achieved unless T_{in} is much higher, and beyond the 420 K limit of the experiments

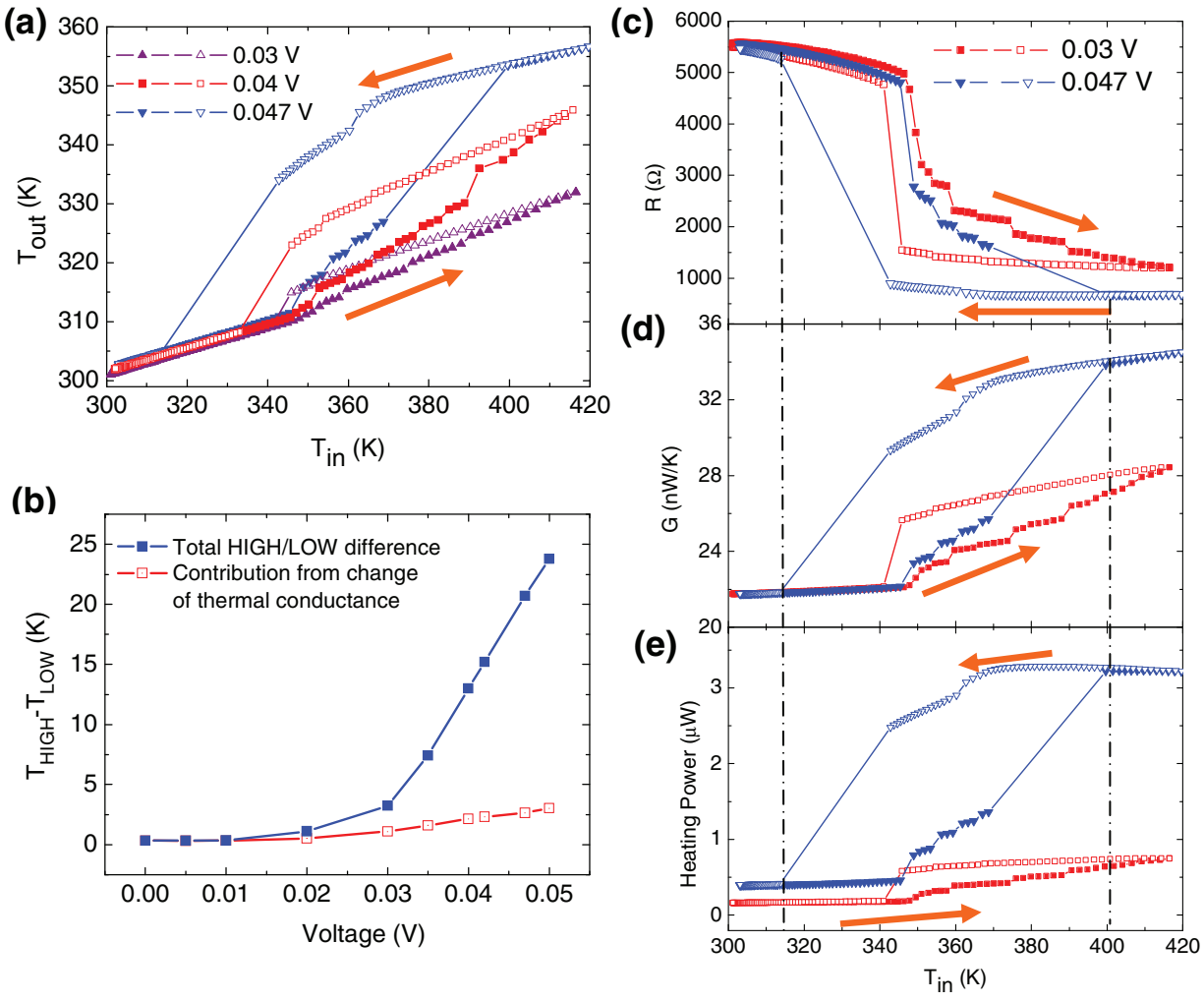

Figure 2. Electrical tuning of the characteristics of the thermal memory under different voltage biases. (a) T_{out} as a function of T_{in} upon heating (filled symbols) and cooling (open symbols). (b) Total HIGH/LOW difference (blue curve) and contribution from the thermal conductance (red curve) at T_{in} = 360 K as a function of the voltage bias. (c) Electrical resistance R, (d) estimated thermal conductance G based on Wiedemann-Franz law, and (e) local Joule heating power as a function of T_{in} upon heating (filled symbols) and cooling (open symbols). Arrows on the curves denote the temperature sweep directions.

carried out. When the voltage bias is increased to 0.05 V, a HIGH/LOW temperature difference can be enhanced to ~25 K at T_{in} = 360 K, two orders of magnitude larger than the case without a voltage bias (blue curve, Figure 2b).

Changes in either thermal conductance or local Joule heating during MIT can alter the temperature profile of the VO_2 nanobeam, and thus the output HIGH/LOW difference. To quantitatively understand the enhancement mechanism, we measured the electrical resistance of the VO_2 nanobeam while simultaneously sweeping T_{in} under different voltage biases (Figure 2c). When Joule heating was applied to the nanobeam, Equation 1 is invalid for calculating the thermal conductance of the nanobeam sample. As indicated in Figure 1f, the change in the phonon contribution G_{ph} to the thermal conductance is negligible in the vicinity of MIT. Therefore, it is reasonable to estimate the change in thermal conductance from the electronic contribution G_e based on the WF law.[11] The corresponding thermal conductance and local Joule heating power of the VO_2 nanobeam are shown in Figure 2d and Figure 2e, respectively, where the thermal conductance was estimated by summing the phonon contribution G_{ph} (middle curve in Figure 1f) and the electronic contribution G_e which was estimated based on the electric resistance from the WF law.[11] As shown in Figure 2d, at 0.047 V, when T_{in} is increased above 400 K, the thermal conductance has increased by ~13.0 nW/K due to the electronic contribution to the heat conduction, leading to a remarkable increase of ~60% in total thermal conductance. This high thermal conductance state is retained upon cooling until T_{in} decreases to ~315 K due to the hysteretic MIT, yielding an enhanced hysteresis loop in the thermal conductance of the VO_2 nanobeam (Figure 2d). The contribution from the change of thermal conductance to the HIGH/LOW difference can be obtained as

$$T_{HIGH} - T_{LOW} = \left(\frac{G_{HIGH}}{G_{HIGH} + G_b} - \frac{G_{LOW}}{G_{LOW} + G_b}\right) T_{in} \quad (2)$$

where G_b is the thermal conductance of the SiN_x beams at T_{in}, G_{LOW} and G_{HIGH} are the thermal conductance of the nanobeam at T_{in} in the heating and cooling process, respectively. As shown by the red curve in Figure 2b, when the voltage bias is increased to 0.05 V, the HIGH/LOW difference attributed to the thermal conductance is enhanced to ~2.5 K at T_{in} = 360 K, representing ~10% contribution to the total HIGH/LOW difference. In other words, the change in local Joule heating of the VO_2 nanobeam can dominant and account for as much as ~90% of the total HIGH/LOW difference (Supporting Information Figures S4 and S5).

To determine the switching performance and repeatability of the thermal memory, we have performed repeated Write HIGH – Read – Write LOW – Read cycles using heating and cooling pulses (**Figure 3**). The temperature T_{in} was initially set to a baseline of 360 K by passing appropriate DC current to the Pt heater at the input terminal. To write a HIGH temperature state to the output terminal, a heating pulse, generated by increasing the heating current was applied to the input terminal to set T_{in} to 435 K. To switch the output terminal to a LOW temperature state, a cooling pulse was applied to the input terminal to set T_{in} to 300 K by natural cooling of T_{in} to the substrate temperature T_{base}. When T_{in} was returned to 360 K for reading, the HIGH (LOW) state of ~332.1 ± 0.1 K (317 ± 0.8 K) was retained and could be read out at the output terminal. It should be noted that the heating current at the input terminal was adjusted accordingly to keep T_{in} at a constant temperature (360 K) in Write and Read cycles. Repeated cycling over 150 times shows that both HIGH and LOW states are reliable and repeatable without degradation, with a slight fluctuation within a range of ±0.8 K in the LOW output state due to small instabilities during the dynamic MIT of the nanobeam.

With the availability of both nonlinear thermal control and nonlinear electrical control, the understanding gained here further allows us to tune the properties and add further unique functionality into the thermal memory through design of the thermal circuit. One interesting yet simple example is a thermal Schmitt trigger by using T_{base} as an input control parameter (denoted as T_1), while both T_{out} and T_{in} are kept at the roughly same temperature, and serve as the output parameter (denoted as T_2) (see inset in **Figure 4**b). As shown in Figure 4a, upon heating under the voltage bias, a very tiny change in T_1 (0.01 K) leads to a drastic change in T_2, due to the single-domain behavior of the suspended VO_2 nanobeam under a positive electrothermal feedback. At a voltage bias of 0.04 V, the positive transition slope $\Delta T_2/\Delta T_1$ is calculated to be ~1450. Further increasing the voltage bias can increase $\Delta T_2/\Delta T_1$, and shift the positive transition edge markedly to the lower temperatures (Figure 4b). When the voltage bias is above 0.13 V, the rising edge appears below the room temperature (not shown here). These observations suggested that the operating temperature of the thermal memory can extend into the cryogenic temperature range, while keeping the local temperature of the VO_2 nanobeam just below the transition point (~340 K) using a higher voltage bias. The extremely sharp trigger transition combined with the tunable operating temperature makes this configuration also very attractive for developing ultrasensitive sensors, such as edge triggered calorimeters and bolometers over a wide range of temperatures.[13]

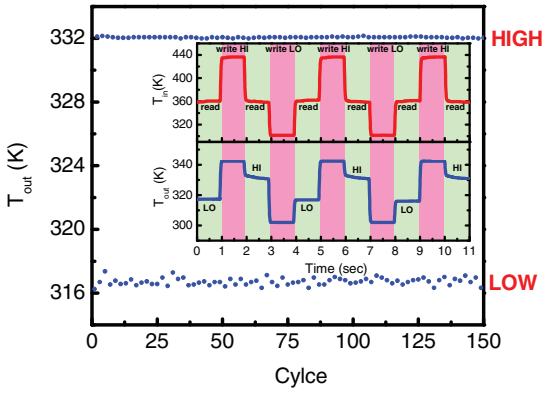

Figure 3. HIGH/LOW (HI/LO) temperature states over 150 repeated cycles by using a one-second heating pulse (435.0 ± 1.0 K) and a one-second cooling pulse (natural cooling to the substrate temperature T_{base} = 300 K) at the input terminal under a voltage bias of 0.04 V. The inset shows the process of Write HI–Read–Write LO–Read over three cycles. After each writing process, the input terminal T_{in} was maintained at 360.0 ± 1.0 K and the output terminal T_{out} was read out.

3. Conclusions

The successful demonstration of a solid-state thermal memory with highly-differentiated HIGH/LOW temperature states

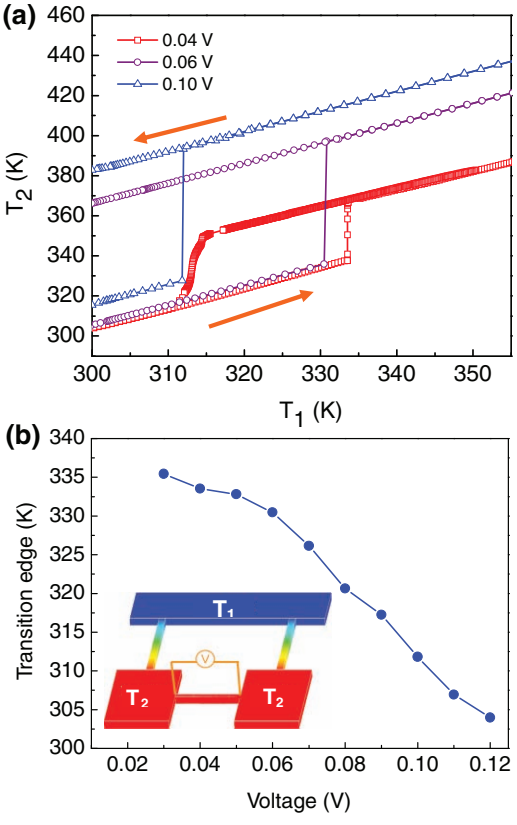

Figure 4. A thermal Schmitt trigger based on the thermal memory device. (a) T_{out} as a function of T_{in} under different voltage biases upon heating and cooling. (b) Tuning the transition edge of the VO_2 nanobeam under different voltage bias. The inset in (b) shows the configuration of the thermal Schmitt trigger.

suggests that it is now possible to realize a practical nonlinear thermal device for storage of information with heat. The incorporation of electrical control onto the VO_2 nanobeam enables remarkable improvements in our ability to tune the heat conduction (~60%) and enhancement of thermal states (two orders of magnitude increase in HIGH/LOW difference). The single-domain behavior of the suspended VO_2 nanobeam provides the greatly improved reproducibility and sensitivity of the thermal devices. In contrast to previously proposed theoretical thermal memory that require complex coupling of nonlinear atomic lattices that are difficult to achieve practically,[3] the experimental approach demonstrated here, utilizing the MIT of the VO_2 nanobeam to obtain nonlinear response, can be readily implemented and precisely controlled. Moreover, it can also be extended to other MIT materials for the exploration of a rich variety of applications,[14] ranging from phononic information processing, smart thermal management, thermal energy storage, and ultrasensitive sensors.

4. Experimental Section

VO_2 Nanobeam Synthesis: We synthesized VO_2 nano- and microbeams via conversion-evaporation and condensation route using V_2O_5 powder (Sigma Aldrich) as source material. The synthesis was carried out in a horizontal tube furnace in flowing Ar carrier gas (99.9%). A porcelain boat loaded with V_2O_5 powder (~0.2 g) was kept inside a quartz tube of diameter ~1.5 cm. Cleaned <100> Si wafer (0.5 cm × 0.5 cm) were placed downstream inside a quartz tube ~ 1–3 cm away from the source powder. The quartz tube was loaded inside the ceramic tube of the furnace with the source powder at the high temperature zone. The ceramic tube was evacuated to a base pressure of 1×10^{-2} mbar before flowing Ar gas at a rate of 300–500 sccm and the pressure was regulated and maintained at ~2 mbar. The temperature of the furnace was ramped to ~870 ± 20 °C at a rate of 20 °C/min. The system was maintained at 870 ± 20 °C for typically 1–2 hours before natural cooling to room temperature.

Thermal Memory Device Fabrication and Thermal/Electric Measurements: The platform for the thermal memory devices and the measurement of thermal conductance is based on a suspended micro-electrothermal measurement device.[9] The schematic and configuration for the measurement of thermal memory properties are shown in Figure S1. The two suspended membranes, integrated with Pt resistive loops serving as both heater and sensor, are branched out with a total of twelve Pt leads supported by twelve suspended SiN_x beams (2 μm in width and 400 μm in length) to the substrate. These 12 Pt leads allows simultaneous 4-probe measurement of the electrical resistance of the Pt loops at the input terminal T_{in} and the output terminal T_{out}, as well as the suspended VO_2 nanobeam in between. The inner two metal contacts also allow us to apply a voltage bias across the VO_2 nanobeam to tune the characteristics of the thermal memory. The temperature is measured based on the resistance of the Pt loops with the use of a sensitive lock-in technique (sensitivity ~ 0.03 K). This method can achieve a sensitivity on the order of 0.1 nW K^{-1} in the measured thermal conductance. To bond the nanobeam onto the four metal contacts, Pt-containing material was deposited at both ends using a focused ion beam at 30 keV and 10 pA (FEI, Quanta 200–3D). During the bonding process, some unavoidable Pt deposition might occur within 1–2 μm away from the irradiated region. We note that this Pt deposition might reduce the intrinsic electrical resistance *R* of the nanobeam. To further improve and stabilize the contacts, annealing was performed by flowing DC current at 200 μA through the nanobeam for 10 min. The voltage bias and DC electrical measurements were conducted using a Keithley 4200 parameter analyzer. The substrate was held at a constant temperature (T_{base} = 300 K) in a vacuum chamber (<1×10^{-5} mbar) using a Janis cryostat, unless otherwise noted.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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